Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Previously Presented) A circuit, comprising:

an input conveying an input signal:

a first pass gate coupled to the input and enabling a first signal in response to the input signal and in response to a master clock signal generating a clock signal;

a first storage node having an input coupled to the first pass gate and having an output storing the first signal:

a second pass gate connected to the output of the first storage node and enabling a second signal in response to the first signal stored on the output of the first storage node and in response to a slave clock signal, wherein the slave clock is a compliment to the master clock signal;

a first inverter connected to the output of the first storage node and generating a first inverted signal in response to the first signal stored on the output of the first storage node;

a third pass gate connected to the first inverter and enabling a third signal in response to the first inverted signal and in response to the slave clock signal; and

an unclocked second storage node having a signal node coupled to the second pass gate and having a complementary signal node coupled to the third pass gate, the signal node storing the second signal and the complementary signal node storing the third signal.

10. (Currently Amended) A circuit as set forth in claim 9, further comprising a second inverter coupled to the second storage node, the second inverter generating an output signal; and a third inverter coupled to the second storage node, the third inverter generating a compliment of the output signal.

11. (Original) A circuit as set forth in claim 10, wherein the first storage node further comprises a fourth inverter and a fifth inverter configured as back-to-back inverters.

12. (Original) A circuit as set forth in claim 11, wherein the second storage node further comprises a sixth inverter and a seventh inverter configured as back-to-back inverters, wherein the sixth inverter is weak relative to the fourth inverter.

13. (Original) A circuit as set forth in claim 10, wherein the second storage node further comprises a fourth inverter and a fifth inverter configured as back-to-back inverters.

14. (Original) A circuit as set forth in claim 13, wherein the fourth inverter is a weak inverter relative to the first inverter.

15. (Currently Amended) A method of operating a differential register, the differential register comprising a first pass gate having a first pass gate data input, a first pass gate enable input, and a first pass gate output; a first storage node having an input coupled to the first pass gate output and having an output; a second pass gate having a second pass gate data input connected to the output of the first storage node and the first pass gate output, a second pass gate enable input, and a second pass gate output; a first inverter having a first inverter input connected to the output of the first storage node and the first pass gate output and a first inverter output; a third pass gate having a third pass gate data input connected to the first inverter output, a third pass gate enable input, and a third pass gate output; a second storage node; an output node; [[,]] and a complimentary output node, the method comprising the steps of:

receiving a data input signal on the first pass gate data input and a master clock signal on the first pass gate enable input;

conveying the data input signal from the first pass gate data input to the first pass gate data output and storing the data input signal on the output of the first storage node when the master clock signal is in a first master clock signal state;

receiving the stored data input signal on the second pass gate input and a slave clock signal on the second pass gate enable input;

conveying the stored data input signal from the second pass gate data input to the second pass gate data output for storage in the second storage node when the slave clock signal is in a first slave cloak signal state, wherein the slave dock signal is a compliment to the master clock signal;

inverting the stored input data signal to generate an inverted stored input data signal;

receiving the inverted stored data input signal on the third pass gate input and the slave clock signal on the third pass gate enable input;

conveying the inverted stored data input signal from the third pass gate data input to the third pass gate data output for storage in the second storage node when the slave clock signal is in the first slave clock signal state; and

on power-up, conveying the stored data input signal stored in the second storage node out of the output node and conveying the inverted stored data input signal stored in the second storage node out of the complimentary output node regardless of states of the master clock signal and the slave clock signal.

16. (Previously Presented) A method of operating a differential register as set forth in claim 15 further comprising the step of conveying the stored data input signal stored in the second storage node out of the output node and conveying the inverted stored data input signal stored in the second storage node out of the complimentary output node in response to settling effects in the storage node.

17. (Canceled)